IN THE CLAIMS:

Please amend the claims as follows:

1.-13. (Cancelled)

14. (Currently amended) A method of forming a multiple-channel semiconductor device, comprising the steps:

forming a stack on a substrate, the stack including at least two lightly doped channel regions vertically separated from each other and from the substrate only by insulator layers, and a single gate electrode located above and separated from the channel regions by an insulator;

forming an oxide liner on sidewalls of the gate electrode;

forming source and drain regions contacting sidewalls of the channel regions; and

forming gate electrode spacers on the oxide liner on the gate electrode.

15. (Original) The method of claim 14, wherein the step of forming an oxide liner includes forming a thermal oxide liner on the sidewalls of the gate electrode.

16. (Currently amended) A method of forming a multiple-channel semiconductor device, comprising the steps:

forming a stack on a substrate, the stack including at least two lightly doped channel regions vertically separated from each other and from the substrate by insulator layers, and a gate electrode separated from the channel regions by an insulator layer;

forming an oxide liner on sidewalls of the gate electrode includes forming a thermal oxide liner on the sidewalls of the gate electrode;

forming source and drain regions contacting sidewalls of the channel regions; and

forming gate electrode spacers on the oxide liner on the gate electrode, ~~The method of claim 15, wherein the step of forming gate electrode spacers on the oxide liner include~~ which

includes depositing nitride on the oxide liner and the gate electrode and performing a spacer etch stopping on the insulator layer separating the gate electrode from the channel regions.

17. (Original) The method of claim 16, wherein the step of forming a stack includes dry etching the insulator layers and the channel regions after the gate electrode spacers are formed, stopping the dry etching on the insulator layer separating the channel regions from the substrate.

18. (Original) The method of claim 17, further comprising implanting source and drain extensions into the substrate after the dry etching.

19. (Original) The method of claim 18, wherein the step of forming source and drain regions includes depositing a lightly doped semiconductor layer over the stack and the gate electrode spacers after the implanting of the source and drain extensions, and depositing a heavily doped semiconductor layer over the lightly doped semiconductor layer.

20. (Original) The method of claim 19, wherein the step of forming source and drain regions further includes dry etching the lightly doped and heavily doped semiconductor layers to form semiconductor spacers on the sidewalls of the channel regions.

21. (Original) The method of claim 20, further comprising forming device spacers on the semiconductor spacers and performing a service and drain implantation into the substrate with the device spacers masking the source and drain extensions.